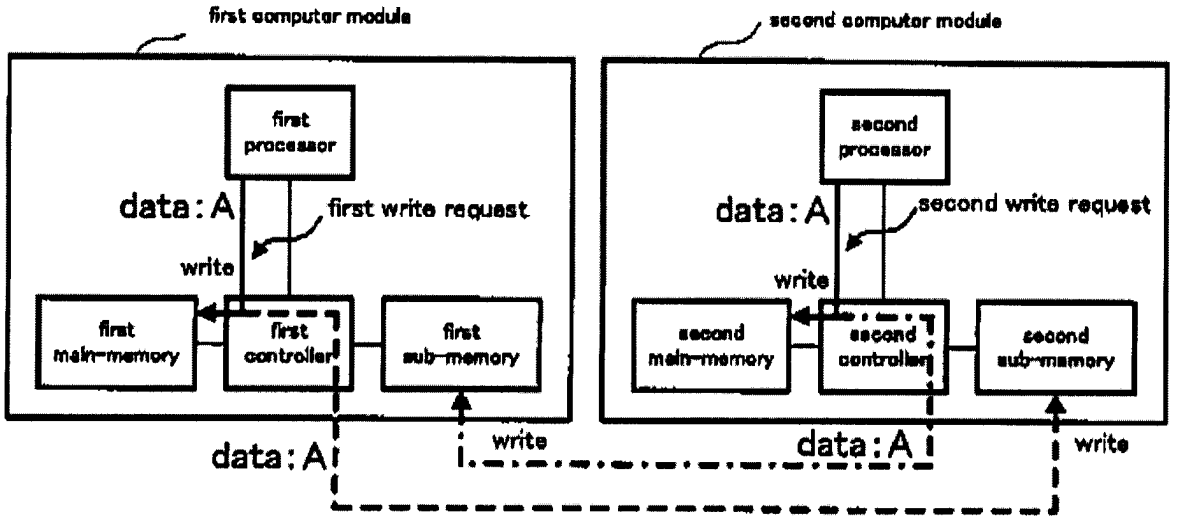
REMARKS

Claims 19-36 are all the claims pending in the application. Claim 37 has been canceled without prejudice or disclaimer.

Claim Rejections

Claims 19-37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Horst et al. (U.S. Patent No. 5,751,932). Claim 37 has been canceled, rendering its rejection moot. Applicants respectfully traverse the rejection of the remaining claims.

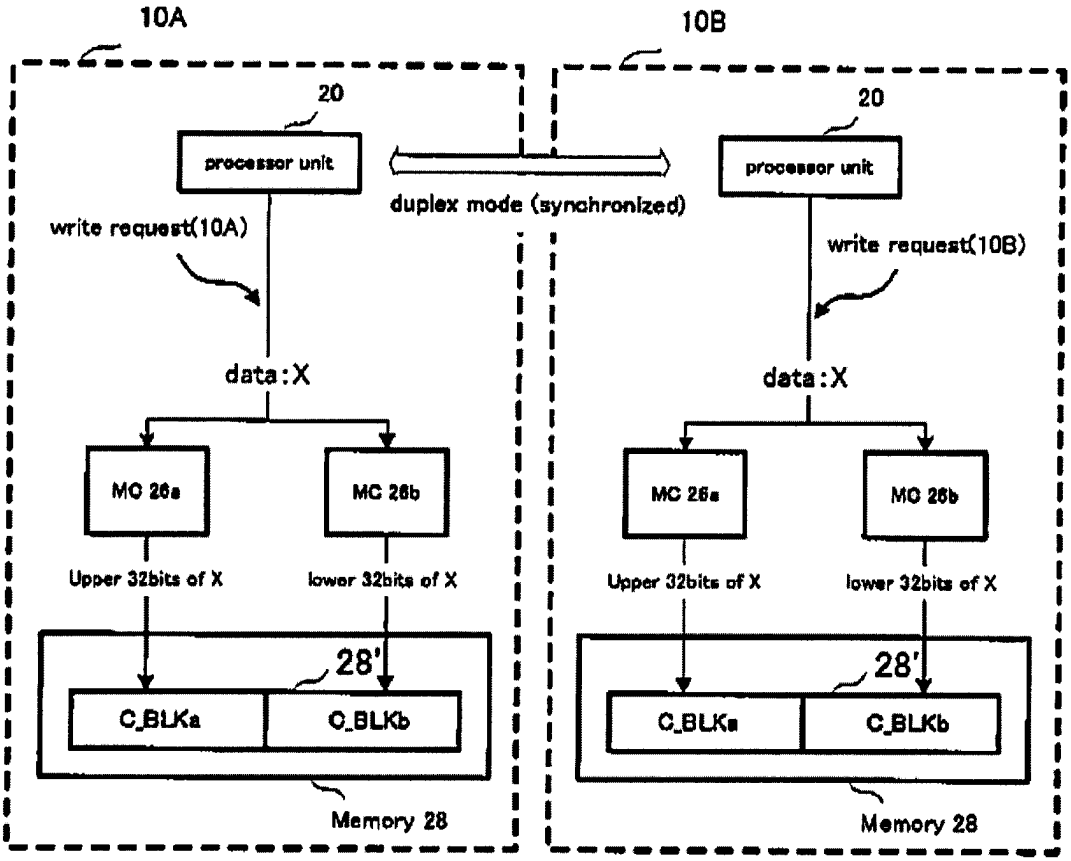
Claim 19 recites, *inter alia*, "said first controller writes data to said first main-memory and said second sub-memory according to a first write request of said first processor, and at the substantially same time, said second controller writes data to said second main-memory and said first sub-memory according to a second write request of said second processor". Accordingly, in the claimed invention, each of the first and second controllers writes data to the main memory of its own computer module and the sub-memory of another computer module according to one write request. Therefore, in a non-limiting exemplary embodiment consistent with claimed invention, even if the processor of one computer fails to be in synchronism, it is possible that each of the sub-memories stores the data which is issued by the processor maintaining the valid operation. A non-limiting example of such an operation consistent with the claimed invention is shown in the chart below.



Explanatory chart for a non-limiting embodiment consistent with the claimed invention

In contrast to the claimed invention, Horst does not disclose a controller which writes data to the memory of its own computer module and the memory of another computer module according to one write request. Horst discloses computer modules 10A and 10B which are synchronized with each other. Memories 28' of the computer modules 10A and 10B each include two regions, C_BLKa and C_BLKb. A processor of the computer module 10A sends a write request to the memory 29 of the computer module 10A (*i.e.*, the processor of the computer module sends a write request to its own memory). The write request is associated with the data (*e.g.*, X), which has 64 bits. A memory controller (MC) 26a of the computer module 10A writes half of the data X (the upper 32 bits) to C_BLKa of the memory 28. A memory controller (MC) 26b of the computer module 10A writes the other half of the data (the lower 32 bits) to the C_BLKb of the memory 28. Processor 20 and MCs 26a, 26b of computer module 10 B operate similarly to the processor and MCs of computer module 10A. So, the memory controllers 26 of

the computer modules 10A and 10B write the data to the memories 28 of the same computer module. (*See* column 29, line 62 through column 30, line 7). An operation of the Horst device is described in the explanatory chart reproduced below. Horst does not disclose the memory controllers 26 writing the data to the memory 28 of its own computer and another computer module according to one write request, as claimed. Accordingly, claim 19 is allowable over Horst. Claims 20-36 depend from claim 19 and are allowable at least by virtue of their dependency.



Explanatory Chart for Horst

Even if Horst discloses that a memory of one of the computers may be written by an external device, it does not disclose that the memories would be written as claimed. Such a general disclosure that a memory may be written to by an outside source clearly does not constitute a disclosure of "said first controller writes data to said first main-memory and said second sub-memory according to a first write request of said first processor, and at the substantially same time, said second controller writes data to said second main-memory and said first sub-memory according to a second write request of said second processor", as recited in claim 19.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Stephen R. Valancius
Registration No. 57,574

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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